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UNITED STATES PATENT APPLICATION

FOR

PHASE INTERPOLATOR

INVENTORS:

DAVID S. DUNNING

CHAMATH ABHAYAGUNAWARDHANA

KEN DROTTAR

RICHARD JENSEN

ROBERT GLENN

PREPARED BY:

KENYON & KENYON

1500 K STREET, N.W.

WASHINGTON, D.C. 20005

(202) 220-4200

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PHASE Interpolator

FIELD OF THE INVENTION

1. Embodiments of the present invention relate to phase interpolators in general and more particularly to such an interpolator useful in recovering a clock from serial data in a tracking receiver.

BACKGROUND OF THE INVENTION

2. In many data communication arrangements, no separate clock signals are transmitted. This requires recovering the clock at the receiving end in order to then recover the data. This can be characterized as the problem , in digital communications, of transferring digital signals between multiple clock timing domains. Multiple clock timing domains include the clock timing domain of a transmitting device as well as the clock timing domain of a receiving device. It is not unusual to transmit digital signals between clock timing domains having nearly the same underlying frequency clock, but different or varying phases with respect to each other.

3. In the prior art, clock recovery circuits provide clock recovery from serial data streams in devices called tracking receivers. Various tracking architectures have been used for this purpose. For example, phase locked loop (PLL) based and delay locked loop (DLL) based tracking architectures have been used. These circuits have various disadvantages. A PLL is an oscillator and injects noise into the surrounding substrate/system. Furthermore, a PLL uses a voltage level to control its oscillation frequency. Hence it is prone to frequency distortions introduced through very low levels of noise on the control lines. A PLL also requires an analog loop filter to damp input noise from interfering with the tracking of the remote transmit clock. This loop filter is an RC time constant network consisting of polysilicon blocks for resistance and gates for capacitance. The analog loop filter consumes a substantial amount of on-die area.

4. Classic DLL based tracking architectures also present problems. These also are prone to frequency distortion introduced through low levels of noise and utilize analog filters which

consume a large on-die area. In addition, a DLL has a finite delay range. A DLL tracks the remote transmit clock by taking a local clock and delaying it until it matches the phase of the remote clock. If the remote clock skews over time or temperature the DLL tracking this clock must add or subtract delay to its local version. If the DLL is asked to delay less than zero, it must add a bit time to that delay to remain within its functional range. Complex circuitry must ignore the additional bit that the adjustment action of the DLL inserts into the recovered data stream. This circuitry must also insert a bit into the recovered data stream when the DLL is asked to delay more than its fixed range.

5. An approach to digital phase interpolation which overcomes some of these disadvantages is disclosed in *Digital Systems Engineering*, 1998, by Dally and Poulton, p. 604-605. The interpolator is described as similar to a typical delay stage but has two differential pairs. In a digitally controlled embodiment, a plurality of digitally controlled tails on each of the differential pairs are provided to select different phases, between two import phases. This avoids some of the problems noted above with PLL and DLL architectures. However, this approach has its own problems. For example, this circuit could require a multiplexer circuit for selecting source clocks. This adds undue additional circuitry and clock distortion during switching. The textbook interpolator also requires a (noise prone) voltage bias to keep the tail current transistors saturated. Furthermore, common mode noise due to charge injection at the nodes between the tail and switching transistors is a problem which is described, but not solved, in the textbook version, when using equally weighted current sources.

6. A need, therefore, exists for a phase interpolator which avoids the problems found in these various prior art architectures.

BRIEF DESCRIPTION OF THE DRAWINGS

7. Fig. 1 is a block diagram of a tracking receiver of the type in which a phase interpolator in accordance with an embodiment of the present invention may be used.

8. Fig. 2 is circuit/block diagram of an embodiment of an interpolation circuit according to the present invention.

9. Fig. 2A is a phase diagram helpful in understanding the operation of the embodiment of Fig. 2.

10. Fig. 3 is a waveform diagram showing phases available in the phase interpolation of the embodiment of Fig. 2

11. Fig. 4 illustrates a number of waveforms helpful in understanding operation of embodiments of the present invention.

DETAILED DESCRIPTION

12. Embodiments of methods and systems for clock recovery are described. In the following description, for purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art, that the present invention may be practiced without these specific details. In other instances, structures and devices are shown in block diagram form. Furthermore, one skilled in the art can readily appreciate that the specific sequence in which methods are presented and performed are illustrative and it is contemplated that the sequences can be varied and still remain within the spirit and scope of the present invention.

13. Fig. 1 is a block diagram of a typical tracking receiver in which embodiments of the phase interpolator of the present invention may be used. Remote serial data on line 11 is input to a phase and frequency detect circuit 13, which has as a second input the recovered remote clock signal on line 15. A control output from block 13, which represents the difference in phase is an input to a remote clock recovery mechanism 17, having as a second input a local reference clock on line 19. The control signal is used to vary the phase of the local reference clock until the recovered clock phase is in a desired frequency and phase relationship with the incoming data.

The recovered clock on line 15 is provided as an output and is used as a clock input to flip-flop 21 which is used to recover the data.

14. Fig. 2 is a circuit/block diagram of an embodiment of phase interpolator according to the present invention. This can be used as the remote clock recovery mechanism 17 in a system such as that of Fig. 2. However, the implementation is Fig. 2 is useful in any arrangement where interpolation between different clock phases is desired. In the illustrated embodiment, from four phases (I, *I, Q and *Q) of a reference clock (also shown on the phase diagram of Fig. 2A), the invention creates one of N phases, indicated by the arrow in Fig. 2A, of that reference clock and its complement as its output. The number of phases that can be created directly corresponds to the size of the digital control, N bits. The example shown in Fig. 2 uses 16 bits of digital control to deliver one of 16 phases of the reference clock and its complement as its output. Depending on requirements, more or fewer than 16 bits may be used. It is also possible to begin with fewer, e.g., 2 or more, e.g., 8 reference clock phases. It will be recognized by those skilled in the art that there is a trade-off between control and precision. The more phases, the more precision and the fewer phases, the simpler the control is.

15. The embodiment of Fig.2, because it uses digital control, is essentially immune to low level noise on the control lines and can exploit a digital loop filter which consumes less on-die area than the analog circuits of the prior art PLL and DLL implementations. None of this additional circuitry is required to implement embodiments of the present invention. Essentially, embodiments of the present invention do digitally what was normally done in analog fashion in the prior art.

16. In the illustrated embodiment four switching "legs" 30, 31, 32 and 33, all tied to common complementary outputs R1, *R1, are provided. Each of the outputs R1 and *R1 of the switching legs 30-33 is coupled to Vcc through a load, 35 and 37 respectively, made up of a pair of transistors in a diode/ triode configuration. A recirculating shift register 39 is used to generate N (in the example 16) phases of the local reference clock. Each switching leg 30-33 includes a differential pair with the drains of the two transistors 41 and 43 coupled together and to ground

through a common tail 50, 51, 52, or 53. In the illustrated embodiment, each common tail includes four equally weighted current sources 55 which are enabled and disabled through digital control by the outputs of the shift register 39. The differential transistors 41 and 43 have on their gates a phase of the reference clock and its corresponding complement.

17. Specifically, in leg 30 transistor 41 has on its gate the in-phase reference clock I and transistor 43 has the inverse thereof. In leg 31, the reference clock quadrature signal Q is provided to transistor 41 and its inverse to transistor 43. Transistor 41 in leg 32 has as its gate input the inverse of I, that is *I and transistor 41 in leg 33 the clock phase *Q.

18. By selectively enabling and disabling current sources, such that only four adjacent are ever enabled it is possible to interpolate between these four phases as shown in Fig. 3. The phase and frequency shift block 13 of Fig. 1 compares data transitions with recovered clock transitions and outputs a signal which shifts the bits in the shift register 39 to change the phase. Thus, embodiments of the present invention provide all phases needed for every phase of interpolation, reducing transistor count and improving noise immunity. The switches 41 and 43 will sum through common output rails 57 and 59 and create phases of the reference clock between those provided by the reference clock. The resultant phase is dependent on the ratio of current sources enabled at each adjacent leg. Thus, with the first four bits of shift register 39 enabling the four transistors 55 in tail 50, the output will be the I phase. As the four bits are shifted the phase will change as shown on Fig. 3. After shifting four places, all four transistors 55 of tail 52 will be enabled and the Q phase will be output. With the four bits as shown in Fig. 2, two transistors 55 in leg 32 and two in leg 33 will be enabled. The interpolated output would be the clock phase 60 of Fig. 3, halfway between *I and *Q.

19. The outputs R and R* can be coupled through "clean up" circuit that is tuned to match the crossing point of the interpolator. Such circuits are well known and typically include an tuned inverter with a P device and N and device with the switching point set by varying gate width so that the inverter switches between logic 1 and logic zero at same point as previous stage so as to avoid distortion.

20. In one particular implementation the circuit is implemented with a 0.16 micron minimum channel length. In this particular embodiment, each transistor size is selected very carefully, as the circuit is tuned to deliver even delay intervals with very low power consumption and high noise immunity. For example, load transistors may be 7/0.32 (w/l), switching transistors may be 30/0.32, and current tails may be 1.3/0.32. They are drawn double minimum length to guarantee some level of uniformity such that each will have equal effect and influence on the circuit. Rule of thumb in these instances is usually triple minimum, however, the circuit would not switch with transistors that size.

21. The embodiment disclosed above uses specific sizes of transistors chosen to behave in the same fashion using a simple digital interface, without additional complexity of voltage bias as in the prior art textbook circuit. Large switching transistors are used to reject some common mode noise due to charge injection at the nodes between the tail and switching transistors, to overcome the problem documented, but not solved in the textbook version, when using equally weighted current sources. In addition, the large switching transistors deliberately load the input clocks such that their rise and fall time are equal to or larger than one quarter of the input clock period.

22. The above-described embodiment uses very small load and current source transistors to reduce the interpolator output to very small (400mv differential) signals. This retains the integrity of the crossing without introducing non-linearities which introduced by the interpolator if signal swung to the extremes of the voltage rails.

23. Fig. 4 shows a comparison of a reference 2.5GHz input waveform to the output as it passes through four stages of 25ps delay (each) in an embodiment such as that described above.

24. Embodiments of the present invention have wide application providing reduced power, area, and pin occupancy in various I/O signaling technologies. These embodiments are applicable to many types of serial interfaces including copper, optical, and chip to chip. Embodiments of the present invention can be used to correct clock skew across a large die, replacing the multiple PLL's which have been used in some applications with the efficiencies and savings mentioned above.

25. For example further noise reduction through addition of a filter on the tail are possible, but not deemed necessary in the illustrated . Furthermore although not necessary in this embodiment, the addition of a "keep alive" current on each current tail would further improve noise immunity by keeping each leg partially enabled.

26. Thus, although several embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.